REMARKS

In the Final Office Action dated September 17, 2004, claims 21-40 are pending and claims 21-40 stand rejected. In this response, claims 21 and 30 have been amended.

Claims 21-40 are provisionally rejected under judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-31 of copending Application No. 09/023,172 and claims 18-30 of copending Application No. 09/023,234. Since this is a provisional rejection, a terminal disclaimer will be submitted when the present application is allowed.

35 USC §112 Rejections

Claim 21 is rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Particularly, claim 21 is rejected for the phrase "direct between", which should have been, "direct interface between", as the Examiner points out in the Office Action. The phrase, "direct between" has been deleted, therefore the rejection is moot.

35 USC §102 Rejections

Claims 21-24, 26, 27, 30-33, 35, 36, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy ("Levy"). In view of foregoing amendment, applicant submits that claims 21-40 are not anticipated by Levy.

Claims 21 and 30 as presently amended claim a memory controller that enables the system bus to interface with a number of different memory devices having a number of different signal quality requirements in relation to each other. Levy, on the other hand

discloses memory modules 30-33 having memory control and timing circuitry 42 that enables the bus 40 to be interfaced **only** to a plurality of magnetic core storage elements 44, 45 (see Col. 6, Lns. 44-47). Levy does not, however, disclose a memory controller in the memory modules 30-33 to interface the bus 40 to any other memory type having any other signal quality requirements than the magnetic core storage elements discussed in column 6, lines 44-47.

Although Levy does discuss that the memory control and timing circuitry 42 can interface the bus 40 to stacks 44, 45 having different **sizes** (Col. 18 Lns. 28-55), Levy does not teach or suggest that the memory control and timing circuitry 42 can interface the bus 40 to varying types of memory having varying types of signal quality requirements, as in presently amended claim 15. Indeed, one of ordinary skill in the art would not equate a memory devices storage capacity with the memory device's signal quality requirements.

Accordingly, it is respectfully asserted by Applicant that presently-amended claims 21 and 30 are not anticipated by Levy and is in condition for allowance.

Claims 25, 28, 29, 34, 37, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy.

In view of the above amendments and arguments regarding claims 21 and 30, it is asserted by Applicant that limitations within claims 25, 28, 29, 34, 37, 38, and 40 are not taught or suggested by Levy, and are therefore not obvious in view of Levy. Accordingly, Applicant respectfully asserts that claims 25, 28, 29, 34, 37, 38, and 40 are in condition for allowance.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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